What Is Claimed Is:

8. A method for using Si-Ge-C in selective etch applications in conjunction with a silicon substrate, comprising:

growing one or more epitaxial layers sequentially, starting at the silicon substrate, wherein at least one of the epitaxial layers comprises Si-Ge-C, wherein the carbon of the Si-Ge-C layer is about 4.5 atomic percent; and

selectively etching the one or more layers adjacent to the Si-Ge-C layer and/or the Si-Ge-C layer wherein the selective etching includes applying a KOH etchant to the Si-Ge-C layer.

10. The method of claim 8, wherein the Si-Ge-C layer etches slower than the one or more adjacent layers.

12. The method of claim 8, wherein the Si-Ge-C layer etches slower than the silicon substrate.

16. A method for using Si-Ge-C in selective etch applications in conjunction with a silicon, germanium, or silicon-germanium substrate, comprising:

growing one or more epitaxial layers sequentially, starting at the substrate, at least one of which comprises Si-Ge-C, wherein carbon is present in the Si-Ge-C layer(s) in an amount sufficient for etch selectivity with respect to the substrate and/or adjacent epitaxial layers; and

etching the one or more layers adjacent to the Si-Ge-C layer or the Si-Ge-C layer or the substrate with HNA, wherein the carbon content is greater than 2 percent.

25. The method of claim 8, wherein the etchant is 10-45 wt% $KOH-H_2O$ and is maintained at a temperature in the range of 50 to 100° C.

27. The method of claim 8, wherein the etchant is 21 wt% $KOH-H_2O$ and is maintained at a temperature in the range of 50 to 100° C.

45. A method of forming a silicon-on-insulator material, the method comprising the steps of:

forming a Si-Ge-C epitaxial layer having a carbon concentration greater than 2 percent, sufficient to function as an etch-stop, wherein the Si-Ge-C resides on a surface of a first semiconductor silicon substrate;

forming a second silicon epitaxial layer on the Si-Ge-C alloy layer;

providing a first oxide layer on a surface of the second epitaxial layer;

providing a second oxide layer on a second semiconductor silicon substrate;

bringing into contact the first and second oxide layers thereby bonding together the first and second semiconductor substrates to thereby form a laminated structure;

removing most of the first silicon substrate;

exposing the laminate to a first etchant which preferentially etches the first silicon substrate until the remainder of the first silicon substrate is removed, but only a part of the Si-Ge-C layer is removed; and

exposing the resultant structure to [a second etchant] HNA which preferentially etches the Si-Ge-C layer for a time sufficient only to remove the remainder of the Si-Ge-C layer thereby producing a silicon-on-insulator material.

47. The method of claim 16 or 45, wherein the carbon is in the range of 4-5 atomic percent.

48. The method of claim 16 or 45, wherein the carbon is about 4.5 atomic percent.

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